AMENDMENT TO THE CLAIMS

1. (Currently Amended) A semiconductor package comprising:

a chip mounting pad having a peripheral edge;

a semiconductor chip attached to the chip mounting pad;

a plurality of leads, each lead including an inner end and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end; and

at least one isolated ring structure disposed along the peripheral edge between the peripheral edge and **all of** the inner ends of the leads in spaced relation thereto, the ring structure being electrically connected to the semiconductor chip and the inner end of at least one of the leads.

2. (Original) The semiconductor package of Claim 1 wherein the inner end of each of the leads is vertically downset with respect to the distal end thereof a distance approximately equal to a thickness of the leads.

3. (Original) The semiconductor package of Claim 1 wherein:

the semiconductor chip includes a chip top surface;

the inner ends each include an inner end top surface; and

the inner end top surfaces are aligned with the chip top surface.

4. (Original) The semiconductor package of Claim 1 wherein:

the ring structure includes a ring top surface;

the inner ends each include an inner end top surface; and

the inner end top surfaces are aligned with the ring top surface.

5. (Original) The semiconductor package of Claim 1 wherein each of the leads further includes a lead transition section disposed between the inner and distal ends thereof.

6. (Original) The semiconductor package of Claim 5 wherein the lead transition section is angularly disposed with respect to the distal end.

7. (Original) The semiconductor package of Claim 1 further comprising a sealing part encapsulating the inner ends of the leads.

8-16. (Cancelled)

17. (Currently Amended) A lead frame comprising:

a frame defining a central opening;

a chip mounting pad disposed within the opening and attached to the frame, the chip mounting pad defining a peripheral edge;

a plurality of leads attached to the frame and extending within the opening toward the chip mounting pad, each of the leads including an inner end disposed in spaced relation to and vertically downset from the chip mounting pad; and

at least one isolated ring structure extending between the peripheral edge of the chip mounting pad and **all of the** inner ends of the leads in spaced relation thereto.

18. (Previously Presented) The leadframe of Claim 17 wherein:

each of the leads has a lead thickness; and

the inner end of each of the leads is vertically downset from the chip mounting pad at a distance approximately equal to the lead thickness.

19. (Previously Presented) The leadframe of Claim 17 wherein:

the ring structure includes a ring top surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the ring top surface.

20. (Previously Presented) The semiconductor package of Claim 17 wherein each of the leads includes a lead transition section extending angularly between the inner end and the frame.

21. (Previously Presented) The leadframe of Claim 17 further comprising at least one temporary connecting bar connecting the ring structure to the chip mounting pad.

22. (Previously Presented) The leadframe of Claim 17 further in combination with a non-conductive connector attached to the ring structure and at least one of the leads for maintaining the ring structure in fixed relation to the chip mounting pad and the leads.

23. (Currently Amended) A semiconductor package comprising:

a chip mounting pad defining a peripheral edge;

a semiconductor chip attached to the chip mounting pad and having a plurality of input/output pads;

a plurality of leads, each of the leads including an inner end and an opposed distal end, the inner end of each of the leads being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset relative to the distal end; and

a means disposed along the peripheral edge between the peripheral edge and **all of** the inner **[[end]] ends** of ~~**each of**~~ the leads for allowing at least two of the input/output pads of the semiconductor chip to be electrically connected to a common one of the leads.

24. (Previously Presented) The semiconductor package of Claim 23 wherein the means comprises at least one isolated ring structure which is electrically connected to at least two of the input/output pads of the semiconductor chip and to one of the leads.

25. (Previously Presented) The semiconductor package of Claim 24 wherein:

the ring structure includes a top ring surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the ring top surface.

26. (Previously Presented) The semiconductor package of Claim 24 wherein:

the semiconductor chip includes a chip top surface;

the inner end of each of the leads includes an inner end top surface; and

the inner end top surface of each of the leads is aligned with the chip top surface.

27. (Previously Presented) The semiconductor package of Claim 1 wherein each inner end of the plurality of leads is generally spaced an equal distance from the peripheral edge.

28. (Previously Presented) The semiconductor package of Claim 1 wherein each inner end of the plurality of leads is positioned outside the at least one isolated ring structure such that there are no lead structures between the at least one isolated ring structure and the peripheral edge.

29. (Previously Presented) The semiconductor package of Claim 1 wherein the at least one isolated ring structure comprises a main body portion oriented substantially parallel and adjacent to the peripheral edge.

30. (Previously Presented) The semiconductor package of Claim 29 wherein the at least one isolated ring structure has a pair of opposing end sections and further comprises a stub portion attached to each end section.

31. (Previously Presented) The semiconductor package of Claim 30 wherein the stub portion is oriented substantially parallel along side one of a plurality of tie bars connected to the peripheral edge of the chip mounting pad.

32. (Previously Presented) The semiconductor package of Claim 17 wherein each inner end of the plurality of leads is generally spaced an equal distance from the peripheral edge.

33. (Previously Presented) The semiconductor package of Claim 17 wherein each inner end of the plurality of leads is positioned outside the at least one isolated ring structure such that there are no lead structures between the at least one isolated ring structure and the peripheral edge.

34. (Previously Presented) The semiconductor package of Claim 17 wherein the at least one isolated ring structure comprises a main body portion oriented substantially parallel and adjacent to the peripheral edge.

35. (Previously Presented) The semiconductor package of Claim 34 wherein the at least one isolated ring structure has a pair of opposing end sections and further comprises a stub portion attached to each end section.

36. (Previously Presented) The semiconductor package of Claim 35 wherein the stub portion is oriented substantially parallel along side one of a plurality of tie bars connected to the peripheral edge of the chip mounting pad.